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Core−Shell Heterostructured Phase Change Nanowire Multistate Memory

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ABSTRACT

Phase-change memory, which switches reversibly between crystalline and amorphous phases, is promising for next generation data-storage devices. In this work, we present a novel, nonbinary data-storage device using core−shell nanowires to significantly enhance memory capacity by combining two phase-change materials with different electronic and thermal properties to engineer different onsets of amorphous-crystalline transitions. Electric-field induced sequential amorphous-crystalline transition in core−shell nanowires displays three distinct electronic states with high, low, and intermediate resistances, assigned as data "0", "1", and "2".

Among various nanowire-based electronic devices fabricated by the bottom-up approach, nanowire memory devices have recently drawn considerable interest with the potential to go beyond the current limitations faced by top-down based fabrication techniques.[1] Advantages of using nanowires for such applications are due to their small sublithographic feature sizes and single-crystalline defect-free structure, where novel functionalities are expected to originate by engineering constituent compositions, sizes, and structures, as in the case of axial,[2–4] radial (core−shell),[5,6] or branched heterostructured nanowires.[7] In most of the nanowire memory devices reported to date, information storage is mainly achieved either by manipulation of small amounts of charges[8] or by charge transfer between organic molecules and inorganic nanowires.[9] Recently, memory devices based on chalcogenide (Ge−Sb−Te alloy) nanowires[10–13] have been reported that satisfy many attributes of "universal memory",[14] such as, fast and reversible memory switching, low power consumption, scalability, and reliable data nonvolatility. The mechanism for the memory switching in phase-change nanowires is fundamentally different from other memory devices; chalcogenide nanowires reversibly undergo amorphous-to-crystalline phase change via electric-field induced Joule heating. These structural transitions lead to distinct electronic states with high/low resistances, which are used to store information in logic circuits.[14,15] For phase-change nanowire memory architectures based on the cross-bar geometry, each cross point of a nanowire with metal electrodes can function as a single active memory cell. In this scheme, the number (N) of nanowires crossed with electrodes represents N bits where each bit is assigned two logic states "0" and "1" due to their amorphous and crystalline phases. These states correspond to conventional binary logic states, where the overall data storage capacity scales as 2^N in an integrated device. This idea further suggests feasibility of nonbinary data storage in phase-change materials and nanowires by utilizing intermediate states between very high (amorphous) and low (crystalline) resistive states in any single memory cell.[16–18] Each distinct logic value can correspond to a different structural state in the electrical programming region. Storage of a particular logic state is enabled by providing electrically induced thermal energy to the phase-change memory device in an amount sufficient to transform the cell to the structural state corresponding to the information. This approach of multistate storage in thin-film based nonvolatile memory device has been previously explored;[19] however, the approach has severe limitations due to difficulties in reliably controlling the precise crystalline/amorphous states, the narrow resistance range for sensing, and the reproducibility. It is possible to overcome these problems by combining phase-change materials with different electrical and thermal properties in heterostructured form such that information can be reliably encoded through the manipulation of the structural state of the constituents, as demonstrated in thin films.[16–18] The utilization of nanowires as memory cells provides unique advantages in realizing high device density in a relatively small integrated structure, benefiting from small diameters of nanowires which are free of etching-induced damage, a common problem with top-down based methods. On the basis of this concept of nonbinary data storage, we present a novel, multistate memory device by configuring core/shell phase-change nanowires comprised of two different phase-change materials, GeTe and $Ge_2Sb_2Te_5$. Through chemical composition

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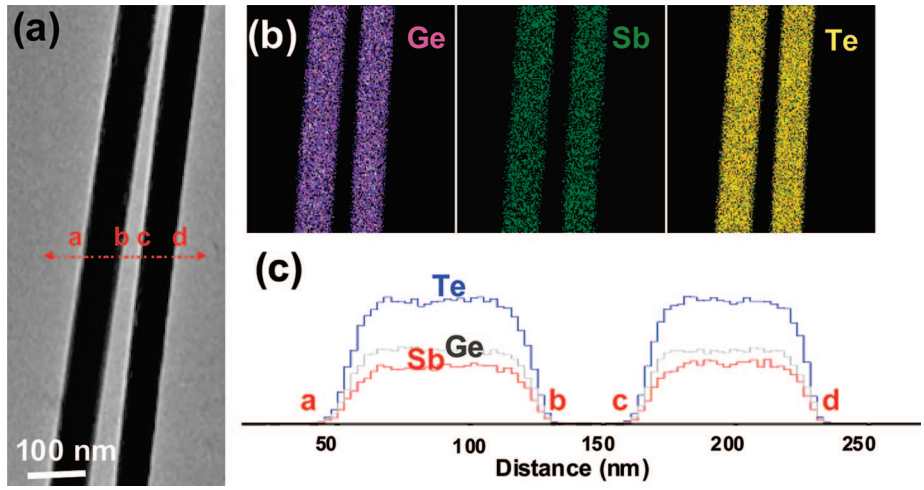

Figure 1. (a) TEM image of two $Ge_2Sb_2Te_5$ nanowires lying on a Cu TEM grid before GeTe deposition. (b) STEM elemental mapping images of the nanowires revealing spatial distribution of Ge, Sb, and Te elements. (c) EDS line scan profile across the red line in (a) shows uniform distribution of each element across the nanowires.

and structural control, we engineer different onsets of amorphous-crystalline transition in $Ge_2Sb_2Te_5$ (core)/GeTe (shell) nanowires to realize an intermediate resistive state between the high/low resistive states upon applying pulsed-electric fields. Three distinct states reversibly switching between low, intermediate, and high resistance values correspond to data storage states "0", "1", and "2", such that overall memory capacity can be significantly enhanced to scale with 3^N.

Core/shell nanowires from different phase-change materials were assembled by growing $Ge_2Sb_2Te_5$ core via the vapor−liquid−solid (VLS) process[20] followed by deposition of a conformal GeTe shell. The synthesis was carried out in two steps. First, the core $Ge_2Sb_2Te_5$ nanowires were synthesized on the basis of the VLS process with our previously reported method.[10,11] $Ge_2Sb_2Te_5$ nanowires were then immediately placed into the growth furnace with GeTe bulk powder inside. The GeTe powder was located at the center of the tube, and the $Ge_2Sb_2Te_5$ nanowires-grown substrate was placed ∼7 in. downstream from the center of the furnace. The temperature of the furnace was raised to 400 °C (substrate temperature ∼190 °C) with a flow of pure Ar gas (100 SCCM) at a vapor pressure of 40 torr. The shell deposition was carried out for two hours, which typically leads to GeTe shelling of ∼50 nm thickness.

The chemical composition of synthesized nanowires was characterized by transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy (EDS) at each stage of the synthesis. Figure 1a is a TEM image of two $Ge_2Sb_2Te_5$ nanowires lying on a carbon-coated Cu TEM grid before GeTe deposition. Scanning TEM (STEM) elemental mapping images (Figure 1b) show the uniform spatial distribution of Ge, Sb, and Te elements throughout the nanowires, which is further confirmed by EDS line scan profile across the same nanowires (Figure 1c). EDS point scanning experiments at arbitrary positions on the nanowires quantitatively confirm that Ge, Sb, and Te are present in an atomic ratio close to 2:2:5 with no phase segregation. As-synthesized $Ge_2Sb_2Te_5$ nanowires are typically single-crystalline possessing either hexagonal[10,11] or cubic[21] crystalline lattices with a 2−3 nm thick native oxide layer often observed on their surfaces, as characterized by high-resolution TEM (HRTEM) and TEM electron diffraction studies (data not shown).

The morphology of $Ge_2Sb_2Te_5$ nanowires after GeTe shell deposition was characterized with TEM and scanning electron microscopy (SEM). The surface of the initial nanowires is roughened after the deposition (Figure 2a, dark-field TEM image), while HRTEM (Figure 2a, inset) shows polycrystalline GeTe is present on the surface. In order to further inspect the internal structure of the GeTe-deposited/$Ge_2Sb_2Te_5$ nanowires, focused ion beam (FIB) milling technique (Ga^+ ion beam, 30 kV and 500 pA) was employed to cut individual nanowires. The SEM image of the FIB-cut GeTe-deposited/$Ge_2Sb_2Te_5$ core−shell nanowire clearly shows that a physical interface (Figure 2b) exists between the core and shell regions throughout the entire length of the nanowire.

The chemical composition of as-synthesized core/shell nanowires was further characterized with STEM-EDS. The STEM elemental mapping image (Figure 2c) reveals the spatial distribution of constituent elements in a core/shell nanowire. Noticeably, Ge is strongly detected away from the core region and is found localized in the shell region, while no obvious spatial variations were detected for other elements. Cross-sectional EDS line scan profile (Figure 2d) from the same nanowire shows a bimodal distribution of Ge, qualitatively consistent with the STEM images. A higher ratio of Ge in the shell region can be understood as follows: the atomic ratio of Ge in the initial, core $Ge_2Sb_2Te_5$ nanowire is ∼22%, while ∼50% of Ge exists in the GeTe deposited on the surface of the initial core nanowire; therefore, a relatively higher concentration of Ge is detected in the GeTe-deposited shell region over the core. Likewise, the relative ratio of Te does not vary much between the core and the shell regions, since ∼55% of Te exists in $Ge_2Sb_2Te_5$ and ∼50% exists in

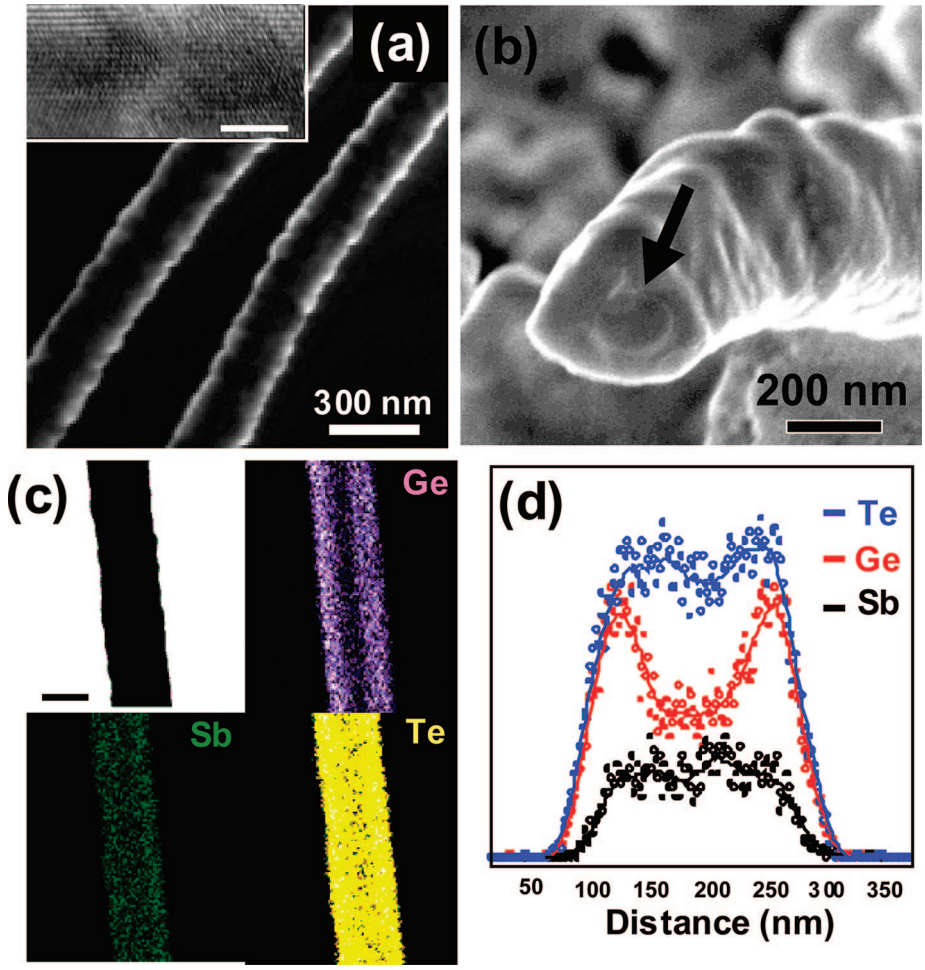

Figure 2. (a) Dark-field TEM image of $Ge_2Sb_2Te_5$ nanowires after GeTe deposition. Inset is a typical HRTEM image of polycrystalline GeTe shell deposited on the surface of $Ge_2Sb_2Te_5$ nanowires. Scale bar; 2 nm (b) SEM image of FIB (Ga^+ ion beam at 30 kV) cross-sectioned $Ge_2Sb_2Te_5$/GeTe−core/shell nanowire. A clear interface between the core and the shell region is visible, as denoted by the arrow. (c) STEM elemental mapping image showing spatial distribution of Ge, Sb, and Te in a $Ge_2Sb_2Te_5$/GeTe−core/shell nanowire. Scale bar; 200 nm (d) cross-sectional EDS line-scan profile of the nanowire in (c) reveals stronger Ge peaks in the shell region.

GeTe. Quantitative EDS analysis indeed confirms that Ge and Te are present in an atomic ratio of 1:1 in the shell region (Supporting Information, S1).

We note that the relative peak heights of each element varies depending on the GeTe deposition time under the same deposition conditions, which reflects the variation in the relative volume portion of the core and shell regions. With longer GeTe deposition times (3.5 h, shell thickness ~80 nm), we often observe uniform distribution of Ge in the EDS profile irrespective of the scanned positions along the nanowire cross section. This qualitatively indicates the relative increase of the volume of GeTe shell over $Ge_2Sb_2Te_5$ core, and the Ge signal in EDS profile is mostly composed of Ge from the GeTe shell. In addition, we also note that some extent of Sb diffusion into the shell region is noticeable, also consistent with a recently reported EDS study on thermal GeTe deposition onto Sb_2Te_3 nanowires,[13] which is most likely due to high volatility of Sb. Nevertheless, we believe that initial composition of $Ge_2Sb_2Te_5$ in the core region is not greatly altered under the current synthesis conditions especially at low temperatures for GeTe deposition. This is strongly supported by our in situ TEM heating experiments on $Ge_2Sb_2Te_5$ nanowires, which show that melting and evaporation of constituent elements and subsequent mass loss from the nanowires are typically observed at temperatures close to 400 °C (data not shown), much higher than the substrate temperature of ~190 °C in the current synthesis conditions. In addition, EDS experiments during the in situ TEM heating indeed confirm that initial composition of $Ge_2Sb_2Te_5$ does not change significantly at ~190 °C, far below the melting temperature. We also note that, while the reaction at lower temperatures can be more efficient in hindering interdiffusion of Sb, it often leads to needle-like, lateral growth of GeTe nanostructures from the surface of $Ge_2Sb_2Te_5$ nanowires, instead of uniform shelling of GeTe (Supporting Information, S2). On the basis of the above analysis, we believe that our synthesis conditions are effective in achieving uniform and conformal deposition of GeTe onto $Ge_2Sb_2Te_5$ nanowires, while maintaining a physically and chemically distinct interface with minimum interdiffusion of the elements.

In control experiments, we often observe that GeTe deposition for a short period of time at higher temperatures, for example, ~560 °C for 1 h (growth substrate temperature:

~340 °C), results in a core/shell nanowire with the reversed spatial distribution of elements, such as, Ge-rich core/Sb−Te rich shell. Even though GeTe deposition is expected on $Ge_2Sb_2Te_5$ nanowires, Ge is typically found localized in the core region, while Sb and Te are predominantly observed toward the outer surface, resulting in Ge-rich core/Sb−Te rich shell deviating from the targeted composition of $Ge_2Sb_2Te_5$ (core)/ GeTe (shell) (Supporting Information, S3). We attribute this reversed elemental distribution to outward diffusion of Sb and Te from the initial $Ge_2Sb_2Te_5$ nanowires during the high-temperature GeTe deposition. Since the deposition occurs at high temperatures, Sb and Te spontaneously diffuse out because of their high volatility (low melting temperature and high vapor pressure),[22] and such diffusion proceeds outward normal to the surface of nanowires possibly due to the internal pressure originating from the curved geometry of nanowires.[23,24] This process is expected to result in a Sb−Te deficient region at the $Ge_2Sb_2Te_5$ core, while higher concentration of Ge (low volatility) is localized in the core. In fact, studies on Ge−Sb−Te thin film devices show that Sb and Te easily undergo thermal diffusion and subsequent phase separation with repeated device operation near the melting temperature, eventually resulting in non-stoichiometric Sb and Te distributions in the active device operation region.[25,26] This is indeed supported by our observations on samples grown for longer GeTe deposition times at the same temperature, such as, ~560 °C for 3 h, which often leads to the localization of Ge both in the shell and in the core with a Ge-deficient interface, while Sb and Te become localized in the shell region only (Supporting Information, S4). These data indicate that, during the high temperature reaction, Sb and Te continuously diffuse out from the $Ge_2Sb_2Te_5$ nanowire core region, while excess Ge diffuses into the core region as well, in addition to being deposited onto the outer surface of the nanowires. Recent studies on the VLS synthesis of Sb_2Te_3 nanowires also report similar Sb−Te tube-like nanostructures,[13] which is consistent with our observations.

Before studying the electrical switching properties of core/shell nanowires in detail, we first compare the memory switching characteristics of single component, GeTe and $Ge_2Sb_2Te_5$ nanowires, since this provides the baseline for interpreting the behavior of core/shell nanowires made from the same constituents. The dc current (I)−voltage (V) behavior of GeTe (Figure 3a, blue curve) and $Ge_2Sb_2Te_5$ (Figure 3a, red curve) nanowires, both of ~110 nm thickness in crystalline states typically display linear $I-V$ behavior[10–12] with low initial resistances of ~2 kΩ for GeTe (unfilled squares) and ~10 kΩ for $Ge_2Sb_2Te_5$ (unfilled triangles) nanowires. The $I-V$ characteristics of the same nanowires amorphized with current pulses (Figure 3a; filled squares for GeTe after 1.7 mA, 100 ns pulse, and triangles for $Ge_2Sb_2Te_5$ after 0.6 mA, 100 ns pulse) displays clear threshold memory switching events (~0.9V for GeTe, and a lower ~0.6V for $Ge_2Sb_2Te_5$) followed by rapidly switching into highly conductive crystalline states. The observation of threshold memory switching indicates phase change between high and low resistive states corresponding to amorphous-crystalline

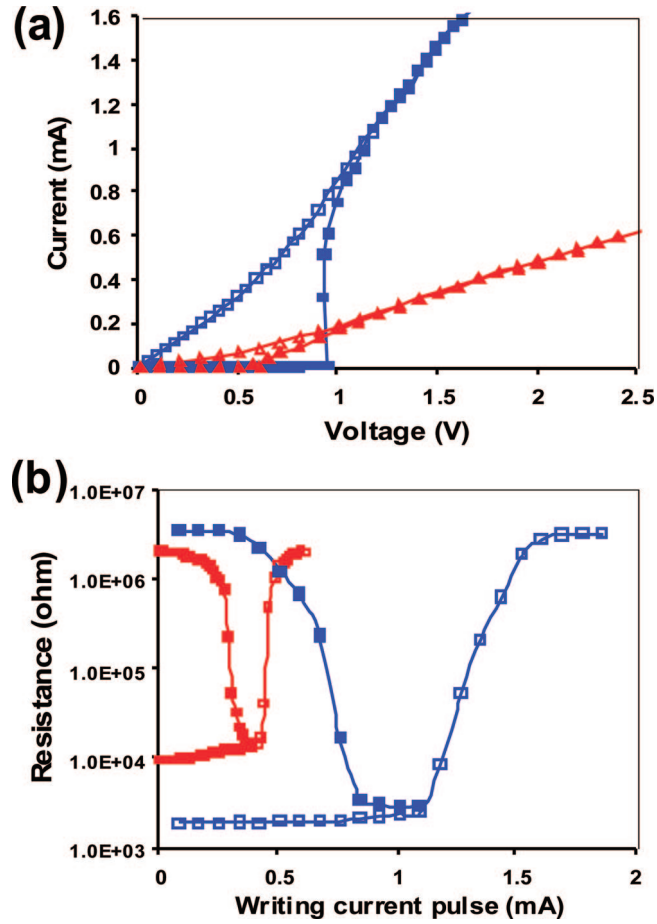

Figure 3. (a) $I-V$ sweep of single-component homogeneous $Ge_2Sb_2Te_5$ (red curve) and GeTe nanowires (blue curve) of ~110 nm thickness in crystalline state (filled symbols) and pulse-induced amorphous state (empty symbols) showing clear threshold switching in both systems (~0.6 V and ~0.9 V respectively). (b) Programming curves, i.e., current-pulse induced resistance variation of the same $Ge_2Sb_2Te_5$ (red) and GeTe (blue) nanowires as a function of increasing pulse amplitude. Filled squares represent the transition from amorphous to crystalline, and empty squares represent the crystalline to amorphous transition.

transition.[10–15] The threshold switching in phase-change materials is known to be governed by a pure electronic mechanism, such as, abrupt carrier generation via electric-field-induced alteration of trapping centers, which does not involve an overall structural transition from amorphous to crystalline.[15,27] In this context, it is speculated that the earlier onset of threshold switching in $Ge_2Sb_2Te_5$ over GeTe is related to its lower conductivity activation energy E_a.; an energy barrier for transition from high to low resistive states, usually assumed to be half of the band gap energy[22] (E_a = 0.8 eV for GeTe[28,29] and 0.3 eV for $Ge_2Sb_2Te_5$[15]). However, any in-depth analysis would require detailed information regarding the electronic states of both materials in amorphous states, such as, the trap densities in the band gaps, which are not available in the literature and, may also change for nanowires with high surface to volume ratio.

The programming characteristics (resistance (R)−current (I) behavior) of the same single-component nanowires (Figure 3b; blue curve for GeTe and red curve for $Ge_2Sb_2Te_5$) represents the variation of resistance after applying current

pulses with increasing amplitudes. Nanowires starting in crystalline states (empty squares) display initial low resistances (~3 kΩ for GeTe and ~11 kΩ for $Ge_2Sb_2Te_5$), which drastically increase upon applying amorphization current pulses over certain threshold amplitudes (~1.4 mA for GeTe, and ~0.4 mA for $Ge_2Sb_2Te_5$). This transition is attributed to crystalline-to-amorphous phase change where short pulses (pulse duration; 100 ns) are required to melt and quench the phase-change materials into an amorphous state.[10–15] Similar abrupt changes in resistance is observed with the nanowires initially in amorphous states (filled squares), where initial high resistances (>1 MΩ) drop to low resistances after applying crystallization pulses over the threshold amplitudes (~0.7 mA for GeTe, and ~0.3 mA for $Ge_2Sb_2Te_5$; 300 ns duration). This change is due to amorphous-to-crystalline transition, where longer pulses (300 ns) with lower pulse amplitudes are required.[10–15] The $R-I$ curves clearly define two distinct electronic states of high/low resistances with a resistance ratio of over $\sim 10^2$ between each state, which forms the basis for phase change based binary data storage. In addition, phase change in $Ge_2Sb_2Te_5$ nanowires typically requires current pulses with lower amplitudes (smaller heat energy) than GeTe nanowires. Earlier onset of phase change in $Ge_2Sb_2Te_5$ nanowires over GeTe nanowires of comparable thickness has been confirmed with nanowires of variable thicknesses,[11,12,30] which is most likely due to the lower crystalliation/melting temperatures of $Ge_2Sb_2Te_5$ than GeTe, both in bulk and at nanometer-scale, coupled with its higher resistivity.[30]

In Figure 4, we present the electrical data obtained from ~200 nm core/shell nanowire, and investigate its memory switching characteristics. As-synthesized core/shell nanowires typically show linear $I-V$ behavior with a low initial resistance (~3 kΩ; Figure 4a). Significantly, the dc $I-V$ sweep on the core−shell nanowire after application of amorphization current pulse (2.0 mA, 100 ns) displays well-resolved, two-step threshold switching behavior (black curve in Figure 4a), in sharp contrast to the response from single-component nanowires (Figure 3a). Following the initial high-resistive state (~1 MΩ), the first threshold switching event appears at ~0.6 V followed by the second threshold switching event at ~1.2 V. On the basis of the lower melting temperature and the lower conductivity activation energy of $Ge_2Sb_2Te_5$ over GeTe as discussed above, we attribute the observed two-step threshold switching to the sequential change in the electronic states of amorphous $Ge_2Sb_2Te_5$ core followed by the amorphous GeTe shell to their respective crystalline states. Studies on the stacked geometry of thin films made of two different phase-change materials, such as, $Ge_2Sb_2Te_5/Sb_2Te_3$ double layer thin films,[16] also report similar two-step threshold switching which reflects the resistance change from each thin film layer. The observation of two distinct threshold switchings indicate the presence of an intermediate resistive state, which is critical for configuring phase-change memory devices based on a nonbinary scheme.[16,17] The nanowire eventually recovers its fully crystallized state at an applied voltage above 2.0 V where the $I-V$ curves between the as-synthesized and the amorphized nanowires become completely overlapping. Unlike the distinct threshold switching observed in single component nanowires (Figure 3a), we note that the threshold switching of core/shell nanowires is not too well-resolved. This may be due to the increased defect states (structural vacancies and defects), which can generate a larger number of trapping centers for charge carriers, thereby, increasing carrier recombination rates,[27] possibly due to interdiffusion of constituent elements and consequential structural alteration resulting from the thermal deposition of GeTe.

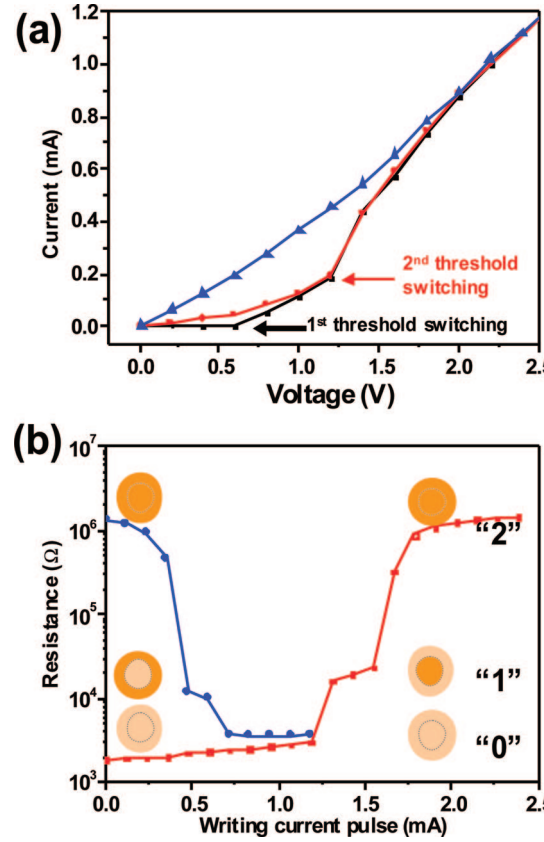

Figure 4. (a) $I-V$ sweep characteristics of a 200 nm $Ge_2Sb_2Te_5$/GeTe−core/shell nanowire device to compare electrical behavior of the nanowire starting from fully crystalline (blue), partially amorphized (red), and fully amorphized (black) states. The two-step threshold switching (marked by arrows) is clearly resolved in the $I-V$ sweep of the fully amorphized nanowire (amorphization current pulse; 2.0 mA, 100 ns). By partially or fully amorphized nanowires, we imply either the core or the shell or both are amorphous locally and not along the entire device length. (b) Variation of resistance of the same core/shell nanowire device as a function of current pulses with varying amplitudes. Pulse durations are 100 ns for amorphization and 300 ns for crystallization. The three different resistive states (low, intermediate, and high) achieved with application of current pulses are clearly distinct. The schematic represent the cross section of the core/shell nanowire at each stage of transition, where color change corresponds to the phase transition: light orange represents crystalline phase, and dark orange is amorphous.

The programming characteristics of the core/shell nanowire (Figure 4b) show three well-resolved resistive states, essential for a nonbinary, multistate memory device; low (2−4 kΩ; data "0"), intermediate (10−30 kΩ; data "1") and high-resistive (>1 MΩ; data "2") states. The highest and lowest resistive states reflect the amorphized and crystallized phases

of the core and shell regions, respectively. Starting from the fully crystalline core/shell nanowire (red curve), abrupt increase of the resistance is observed following a current pulse (100 ns) of ~1.2 mA. This change is attributed to faster amorphization of $Ge_2Sb_2Te_5$ (core) which easily undergoes phase change compared with GeTe (shell) as shown in Figure 3a,b and is consistent with our previous studies.[11,12,30] Here, the overall resistance (~10 kΩ) of the device is due to the remaining crystalline GeTe shell. Since the current now flows predominantly through the crystalline GeTe shell, further increase in the current pulse amplitude eventually induces amorphization of the shell (~1.7 mA) as well, thereby making the core and shell regions amorphous. Similarly, for the nanowire initially in the amorphous phase (blue curve), recrystallization of core $Ge_2Sb_2Te_5$ occurs first followed by that of GeTe shell displaying three-distinct resistance regions, which demonstrates that the multistate programming is a reversible process. Such multilevel resistive states are a unique feature of programming characteristics often realized in stacked thin films of two different phase-change materials, such as, $Ge_2Sb_2Te_5/Sb_2Te_3$[16] and $GeTe/Sb_2Te_3$[18] where each resistive state represents different structural states of the component materials; both (core/shell) crystalline, both amorphous, and, one crystalline while another in amorphous phase.[18]

The presence of an intermediate resistive state (crystalline-core/amorphous-shell) is indeed observed from the dc $I-V$ sweep of the nanowire prepared in the intermediate state (red curve, Figure 4a), where the first threshold switching (black arrow) disappears, while the second threshold switching (red arrow) is retained, confirming the presence of an electrically stable intermediate state with resistance ratios >10 between each state. The earlier onset of recrystallization/amorphization in core $Ge_2Sb_2Te_5$ is well-understood on the basis of the lower crystallization/melting temperatures of $Ge_2Sb_2Te_5$ over GeTe both in bulk and in the nanometer regime which requires lower heat energy for the phase transition.[30]

By focusing on the $R-I$ characteristics, we provide detailed interpretation of the multistate memory switching behaviors of core/shell nanowires. A core/shell nanowire in a cylindrical geometry can be conceptualized as two parallel electrical resistors. In this schematic, the total resistance of a core/shell nanowire (R_{tot}) under applied voltage can be expressed as

$$1/R_{tot} = 1/R_{core} + 1/R_{shell}$$

where R_{core} and R_{shell} represents the resistance of the core and the shell, respectively.

For the case where both core and shell are initially crystalline (red curve in Figure 4b), current flows through the entire cross section of the nanowire, which can be approximated with a resistance as defined above. Once a critical current pulse (~1.2 mA) is applied, amorphization of $Ge_2Sb_2Te_5$ core occurs earlier than that of the GeTe shell, since it requires a lower amount of heat energy mainly due to the lower melting temperature of $Ge_2Sb_2Te_5$ (~616 °C in bulk) than that of GeTe (~725 °C in bulk).[22,30] The amorphization of the core leads to an abrupt increase of R_{core} (over ~100 times),[10,11] while R_{shell} retains its low value (low resistance at crystalline state). The total resistance R_{tot} at this state represents the resistance of the intermediate state (core in amorphous and shell in crystalline states), which is approximately equal to R_{shell} ($1/R_{core}$ is negligibly small compared with $1/R_{shell}$; therefore, $1/R_{tot}$ becomes approximately equal to $1/R_{shell}$). This implies that the intermediate resistance reflects the resistance of the crystalline GeTe shell, through which the current predominantly flows. The increased ratio of R_{tot} (~10) from the initial crystalline to the intermediate state, thereby, reflects the change in the cross-sectional area for carrier transport; the combined cross section of the initially crystalline core and shell is effectively reduced to the cross section of the crystalline GeTe shell only.

In the case where both core and shell regions are initially in amorphous states, (blue curve in Figure 4b), the core, amorphous $Ge_2Sb_2Te_5$ core undergoes recrystallization before the GeTe shell because of its lower crystallization temperature ($Ge_2Sb_2Te_5$ ~140 °C,[31] and GeTe ~ 170 °C[32]), once a certain current pulse amplitude (~0.4 mA) is reached. This leads to a drastic increase of $1/R_{core}$ thereby making $1/R_{shell}$ relatively negligible. Therefore, $1/R_{tot}$ becomes approximately equal to $1/R_{core}$, implying that, at the intermediate state, the total resistance of the core/shell nanowire represents the resistance of core $Ge_2Sb_2Te_5$ in the crystalline state. The observed huge resistance drop (from over ~1 MΩ to ~10 kΩ), thereby, reflects the change in the resistance of $Ge_2Sb_2Te_5$ between amorphous and crystalline states. The resistance ratio of over $\sim 10^2$ is indeed consistent with those observed in pure $Ge_2Sb_2Te_5$ nanowires during amorphous−crystalline phase change.[11]

In addition, it is important to mention that the above analysis is based on the phase transition of $Ge_2Sb_2Te_5$ and GeTe in bulk, and size-dependent materials properties, such as, thermal conductivity or crystallization/melting temperature are not considered. However, as we have previously demonstrated, phase-change phenomenon in $Ge_2Sb_2Te_5$ and GeTe nanowires is very strongly size-dependent;[11,12,30] the reduction of the nanowire cross-sectional area leads to lower required currents for amorphization/crystallization.[11,12,30] Size-dependent phase change in nanowires is mainly attributed to the increased heat localization with scaling down of cross-sectional area of phase-change materials,[33] coupled with reduction of thermal conductivity,[34] activation energy for phase change,[11] and crystallization/melting temperatures.[30] Therefore, the onset of amorphization in core/shell nanowires is dependent on the relative cross-sectional areas of core and shell regions; if the thickness of GeTe shell becomes too thin, then it is expected that the GeTe shell would be amorphized before core $Ge_2Sb_2Te_5$. This situation is not desirable and has been considered in our design of core−shell nanowires, since amorphization of GeTe typically requires more heat energy than $Ge_2Sb_2Te_5$ of comparable thickness.[11,12,30] In fact, we could not obtain multilevel switching in core−shell nanowires with <20 nm GeTe shell. Therefore, there is an optimized range of thickness of the GeTe shell, whereby a large resistance ratio is realized between the crystalline and the intermediate state and accompanied by

lower writing currents to amorphize $Ge_2Sb_2Te_5$ over GeTe. However, more work is required in the future to study the interesting size-dependent properties of core−shell phase-change nanowires.

In conclusion, these studies demonstrate that multistate memory can be reliably achieved from nanoscale components made by self-assembly. Electric pulse induced-sequential amorphous−crystalline transition in core−shell nanowires shows three distinct electronic states with low, intermediate, and high resistances, each assigned as data values, "0", "1", and "2". The nonbinary data encoding in phase-change core−shell nanowires is also significant from the point of view of practical device assembly using nanowires, as now significantly higher memory density can be achieved from relatively fewer nanowires without the need to develop complex schemes to assemble nanowires in large quantities. In addition, the electrical response of the devices can be tuned by changing sizes and chemical compositions thereby opening up interesting possibilities to fabricate practical devices with new features.

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Supporting Information Available: EDS profile, low-magnification TEM image, and STEM mapping images. This material is available free of charge via the Internet at http://pubs.acs.org.

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